Customer No.: 31561
Docket No.:10958-US-PA
Application No.: 10/604,651

In The Claims:

1. (currently amended) A method of forming a low temperature polysilicon thin film transistor, comprising the steps of:

forming an amorphous silicon layer over a substrate;

performing a plasma treatment to the amorphous silicon layer;

transforming the amorphous silicon layer into a polysilicon layer;

patterning the polysilicon layer to form a plurality of island polysilicon layers;

forming a channel region and a doped source/drain region on each side of the channel region in each island polysilicon layer; and

forming a gate over each channel region.

2. (original) The method of claim 1, wherein the step of performing the plasma treatment comprises applying an oxygen-containing plasma to adjust the threshold voltage in the negative direction.

3. (original) The method of claim 2, wherein the oxygen-containing plasma comprises nitrous oxide (N_2O) plasma.

4. (original) The method of claim 1, wherein the step of performing the plasma treatment comprises applying a hydrogen-containing plasma to adjust the threshold voltage in the positive direction.

5. (original) The method of claim 4, wherein the hydrogen-containing plasma comprises ammonia (NH_3) plasma.

6. (original) The method of claim 4, wherein the hydrogen-containing plasma comprises hydrogen (H_2) plasma.

7. (original) The method of claim 1, wherein the desired shift in the threshold voltage is effected by varying the radio frequency power to the plasma treatment.

8. (original) The method of claim 1, wherein the desired shift in the threshold voltage is effected by varying the processing period of the plasma treatment.

9. (original) The method of claim 1, wherein the step of patterning the polysilicon layer further comprises forming a gate insulation layer over the island polysilicon layers.

10. (currently amended) A method of forming a low temperature polysilicon thin film transistor, comprising the steps of:

providing a substrate;

forming an amorphous silicon layer over the substrate;

performing a plasma treatment to the amorphous silicon layer;

performing a laser annealing process to transform the amorphous silicon layer into a polysilicon layer;

patterning the polysilicon layer to form a plurality of island polysilicon layers;

forming a gate insulation layer over the island polysilicon layers;

forming a channel region in each island polysilicon layer and a doped source/drain region on each side to the channel regions; and

forming a gate over the channel regions.

11. (original) The method of claim 10, wherein the step of performing the plasma treatment comprises applying an oxygen-containing plasma to adjust the threshold voltage in the negative direction.

12. (original) The method of claim 11, wherein the oxygen-containing plasma comprises nitrous oxide (N_2O) plasma.

13. (original) The method of claim 10, wherein the step of performing the plasma treatment comprises applying a hydrogen-containing plasma to adjust the threshold voltage in the positive direction.

14. (original) The method of claim 13, wherein the hydrogen-containing plasma comprises ammonia (NH_3) plasma.

15. (original) The method of claim 13, wherein the hydrogen-containing plasma comprises hydrogen (H_2) plasma.

16. (original) The method of claim 10, wherein the desired shift in the threshold voltage is effected by varying the radio frequency power to the plasma treatment.

17. (original) The method of claim 10, wherein the desired shift in the threshold voltage is effected by varying the processing period of the plasma treatment.

18. (original) The method of claim 10, wherein the laser annealing process comprises performing an excimer laser annealing process.

19. (original) The method of claim 10, wherein the step of forming the amorphous silicon layer over the substrate, further comprises:

forming a silicon nitride layer over the substrate; and

forming a silicon oxide layer over the silicon nitride layer.

20. (original) The method of claim 10, wherein the step of forming a channel layer in each island polysilicon layer and a doped source/drain region on each side to the channel region further comprises:

forming a first patterned photoresist layer over the gate insulation layer to expose the upper surface of on each side of each island polysilicon layer; and

performing a p^+ doping process.

21. (original) The method of claim 20, wherein the step of performing the p^+ doping process further comprises removing the first patterned photoresist layer.

22. (original) The method of claim 10, wherein the step of forming a channel region in each island polysilicon layer and a doped source/drain region on each side to the channel region further comprises:

forming a second patterned photoresist layer over the substrate to cover a portion of the various island polysilicon layers and expose the upper surface on each side of the island polysilicon layers; and

performing an n^+ doping process.

23. (original) The method of claim 22, wherein the step of performing the n^+ doping process further comprises removing the second patterned photoresist layer.

24. (original) The method of claim 23, wherein the step of removing the second patterned photoresist layer further comprises:

forming a third patterned photoresist layer over the gate insulation layer to expose an area adjacent to the doped source/drain region of various island polysilicon layer; and

performing an n^- doping process to form lightly doped drain regions.

25. (original) The method of claim 24, wherein the step of performing the n^- doping process further comprises removing the third patterned photoresist layer.

26. (original) The method of claim 10, wherein the step of forming a gate over the channel regions further comprises performing an activation process.

27. (original) The method of claim 10, wherein the step of forming a gate over the channel regions further comprises:

forming an inter-layer dielectric over the substrate;

forming a plurality of first openings in the inter-layer dielectric and the gate insulation layer to expose the doped source/drain regions; and

forming a plurality of source/drain metallic contacts over the inter-layer dielectric so that the source/drain metallic contacts and various doped source/drain regions are electrically connected via the first openings.

28. (original) The method of claim 27, wherein the step of forming a plurality of source/drain metallic contacts further comprises:

forming a passivation layer over the substrate;

forming a second opening in the passivation layer to expose a portion of the source/drain metallic contact; and

forming a pixel electrode over the passivation layer such that the pixel electrode and a portion of the source/drain metallic contact are electrically connected through the second opening.

Claims 29-39 (cancelled)